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# *GBT-FPGA Firmware Starter Kit for Altera and Xilinx devices*

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## Version History

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V0.0	26/01/10	Sophie Baron	Creation
V0.1	26/02/10	Sophie Baron	Update on compilation process

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## Introduction

### GBT-FPGA aim

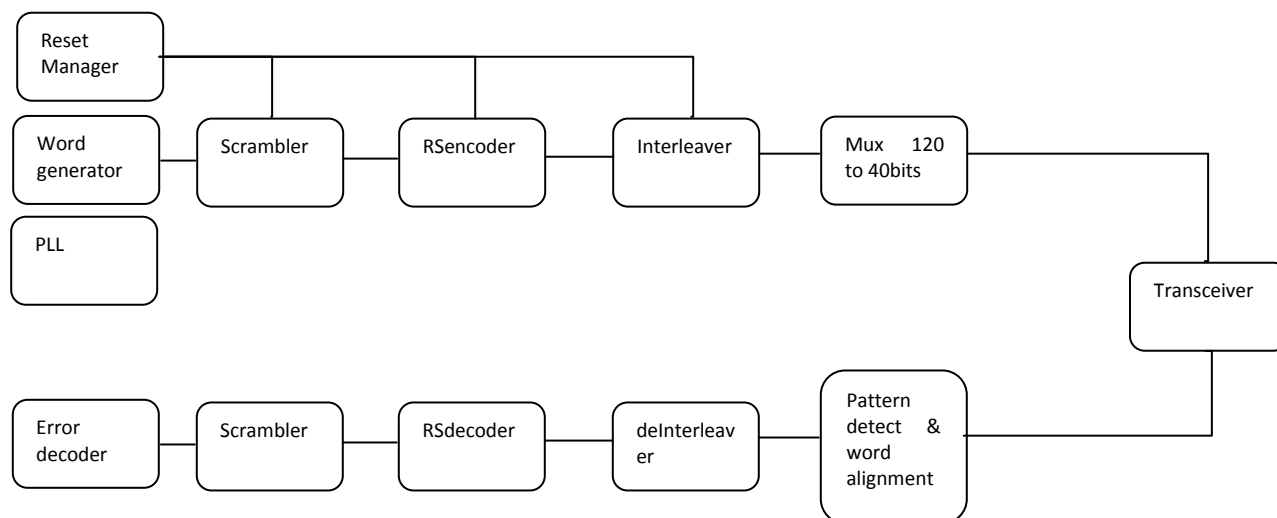
The GBT chip is a radiation tolerant ASIC that can be used to implement bidirectional multipurpose 4.8Gb/s optical links for high-energy physics experiments. It will be proposed to the LHC experiments for combined transmission of physics data, trigger, timing, fast and slow control and monitoring. Although radiation hardness is required on detectors, it is not necessary for the electronics located in the counting rooms, where the GBT functionality can be realized using Commercial Off-The-Shelf FPGAs.

Having a transposition of the GBTserdes chip into FPGAs would thus be very useful, not only for the counting room GBTs, but also to emulate the GBT chip before its actual release, and to design test platforms for GBT testing and system validation. A team located in Marseille (CPPM) and at CERN implemented the GBT protocol in Altera and Xilinx FPGAs and made it available to users via SVN.

The current implementations are based on Altera StratixIIGX and Xilinx Virtex5 and will progressively be completed with StratixIV and Virtex6 designs and optimization techniques. They constitute a Firmware Starter Kit to get familiar with the GBT protocol.

### GBT-FPGA code

The GBT-FPGA Starter Kit provides a set of blocks in charge of each step of the GBT serialization-deserialization procedure, coded in the most generic way. Very simple word generator and error detection blocks are provided to allow a simple standalone link test. Most of these blocks are common for Altera and Xilinx designs. However, a few blocks had to be designed using vendors core generators: PLLs, Transceivers and dual-port RAMs. One version of these blocks is provided per Vendor and per Chip.



All the sources are available (except the IP cores, of course), and the users are free to modify them if needed.

## Project Structure and Files Organization

The Starter Kit is available for download to any GBT user, provided that he makes the request to [sophie.baron@cern.ch](mailto:sophie.baron@cern.ch). He will thus be granted a read access to the GBT-FPGA site, and in particular to the [Starter Kit Firmware Release page](#), where the latest versions of the starter kit as posted as a .rar file.

## SVN repository

The GBT-FPGA Starter Kit is also posted on the following SVN repository.  
[https://svnweb.cern.ch/cern/wsvn/gbt\\_fpga/starter\\_kit/#path\\_starter\\_kit](https://svnweb.cern.ch/cern/wsvn/gbt_fpga/starter_kit/#path_starter_kit)  
[ / ] [ Starter\_kit/ ] [ version-1.0.0/ ] [ sources/ ] - Rev 127

### LAST MODIFICATION

Rev 125 2010-02-26 15:14:20

Author: sspriet

Log message:

added tx\_dp\_ram and RX\_dp\_ram to the Xilinx version of demu and mux

Path

branches/

Starter\_kit/

version-1.0.0/

doc/

projects/

sources/

bert/

control/

eports/

plls/

serdes/

tags/

trunk/

Compare Paths

Each registered user has a read access to this repository, and can get a working copy of the Starter Kit.

## Starter Kit Architecture

The Starter Kit is a set of sources organized in 3 folders: DOC, PROJECTS and SOURCES:

- DOC: contains this document
- PROJECTS: is organized as follows

ALTERA	STRATIXIIGx	Top_file.vhd Constants.vhd Project files (qpf, qsf)
	STRATIXIVGx	
XILINX	VIRTEX5	Top_file.vhd Constants.vhd Project files (ise, ucf, tcl...)
	VIRTEX6	

One project has been created and compiled for a component of each family, tested on one evaluation board. All the projects are using the same set of source files, all located in the ***sources*** folder, the only difference being the vendor related entities (transceivers, plls, rams). For each project, the list of files is carefully made to call the right entities.

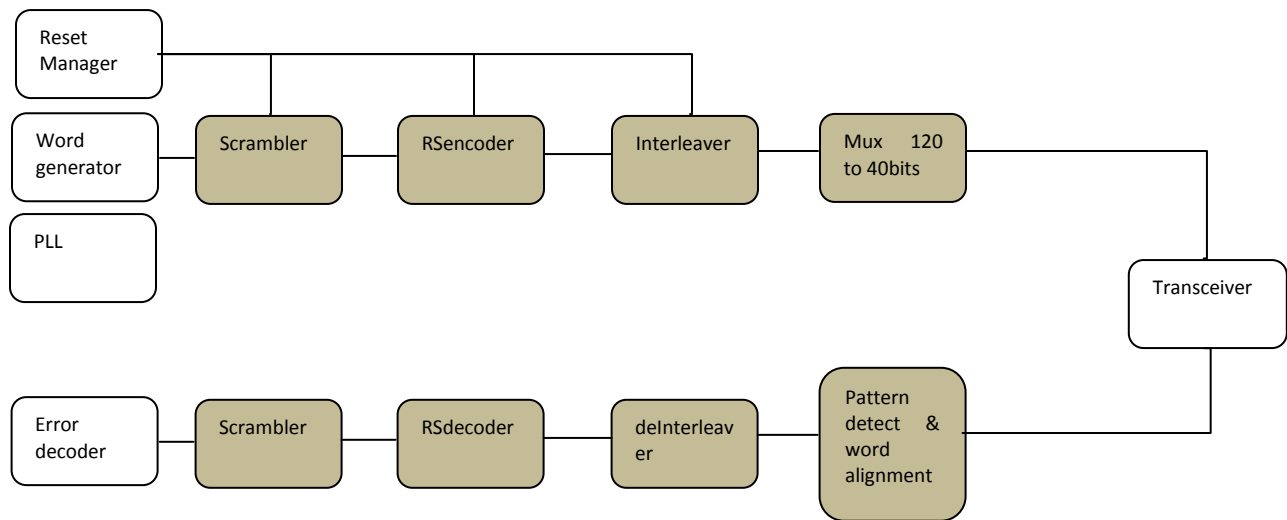
- **SOURCES:** These files are all available in this folder. They are organized by functionality.

BERT				Error_detection_module.vhd	
CONTROL				Word_generator.vhd	
EPORTS				Reset_manager.vhd	
				-	Will contain the blocks relative to e-port for full GBT emulation
PLLS	ALTERA	STRATIX IIGx		Pll.vhd	
	XILINX	VIRTEX5		Pll.vhd	
SERDES	BASICS			Agnostic_21bits_counter.vhd	
				Gf16add.vhd	Function used both by RS enc and RS dec
				Gf16mult.vhd	
	DESERIALIZER	DEINTERLEAVE		Reverse_interleaving.vhd	
		DEMUX40_to_120 bits		Read_RX_DPRAM.vhd	
		ALTERA		Demux_40_to_120bits.vhd	Entity instantiating the IP core
				Rx_dp_ram.vhd	IP core
		XILINX	VIRTEX5	Demux_40_to_120bits.vhd	Entity instantiating the IP core
				Rx_dp_ram.vhd	IP core
		DESCRAMBLER		Descrambler.vhd	
				Descrambling.vhd	
		MANUAL_FRAME_ALIGNMENT		Manual_Frame_Alignment.vhd	
				Modulo_40_Counter.vhd	
			Right_Shifter_39b.vhd		
			Write_Rx_dp_ram.vhd		
	PATTERN_SEARCH		Pattern_Search.vhd		
	RSDECODER		Adder60.vhd		
			ChienSearch.vhd		
			Decoding.vhd		
			Errorlocpolynomial.vhd		
			Gf16inverse.vhd		
			Gf16log.vhd		
			Gf16shifter.vhd		
			Lambdadeterminant.vhd		
			RSDecoder.vhd		
			RSTwoErrorCorrect.vhd		
			Syndromes.vhd		
	OPTIMIZATION_UTILITIES			Frame_TDD_x2.vhd	Time Division Demultiplexer for optimization x2
				Frame_TDD_x3.vhd	Time Division Demultiplexer for optimization x3
				Frame_TDD_x4.vhd	Time Division Demultiplexer for optimization x4
				Frame_TDM_x2.vhd	Time Division Multiplexer for optimization x2
				Frame_TDM_x3.vhd	Time Division Multiplexer for optimization x3
		Frame_TDM_x4.vhd	Time Division Multiplexer for optimization x4		
SERIALIZER	INTERLEAVE		Interleaving.vhd		
	MUX_120_to_40bits		RW_tx_dp_ram.vhd		
	ALTERA		Mux_120_to_40bits.vhd	Entity instantiating the IP core	
			Tx_dp_ram.vhd	IP core	
	XILINX	VIRTEX5	Mux_120_to_40bits.vhd	Entity instantiating the IP core	
			Tx_dp_ram.vhd	IP core	
	RS_ENCODER		Encoding.vhd		
			Polydivider.vhd		
			RSencoder.vhd		
	SCRAMBLER		Scrambler.vhd		
		Scrambling.vhd			
		Scrambling_constants.vhd			
TRANSCIEVER	ALTERA	STRATIX IIGX STRATIX IVGX	GX_serdes.vhd		
	XILINX	VIRTEX5 VIRTEX6			

VHDL file wrapping the vendor specific core  
Vendor specific core, briefly described below

## Serdes

The serializer folder includes all the blocks and entities required to serialize and deserialize the data:



## Compiling the downloaded projects

### Altera

To recompile the project with quartus II (we are working with Quartus II 9.0 SP2), open the project Enc\_Ser\_Des\_Dec.qpf in Projects/Altera/StratixIIgx/resource\_optimization\_with\_multi\_links and compile directly. All the required files are normally already added to the project and it should be straight. Please note that the compilation is set for the device EP2SGX90FF1508C3 and the power/pin assignments for the evaluation board type PCIe SIIGX Dev Kit. Be careful to redefine the power and pin assignments according to your own design.

Typical connection of the PCIe SIIGX Dev Kit to test the GBT-FPGA Starter Kit:

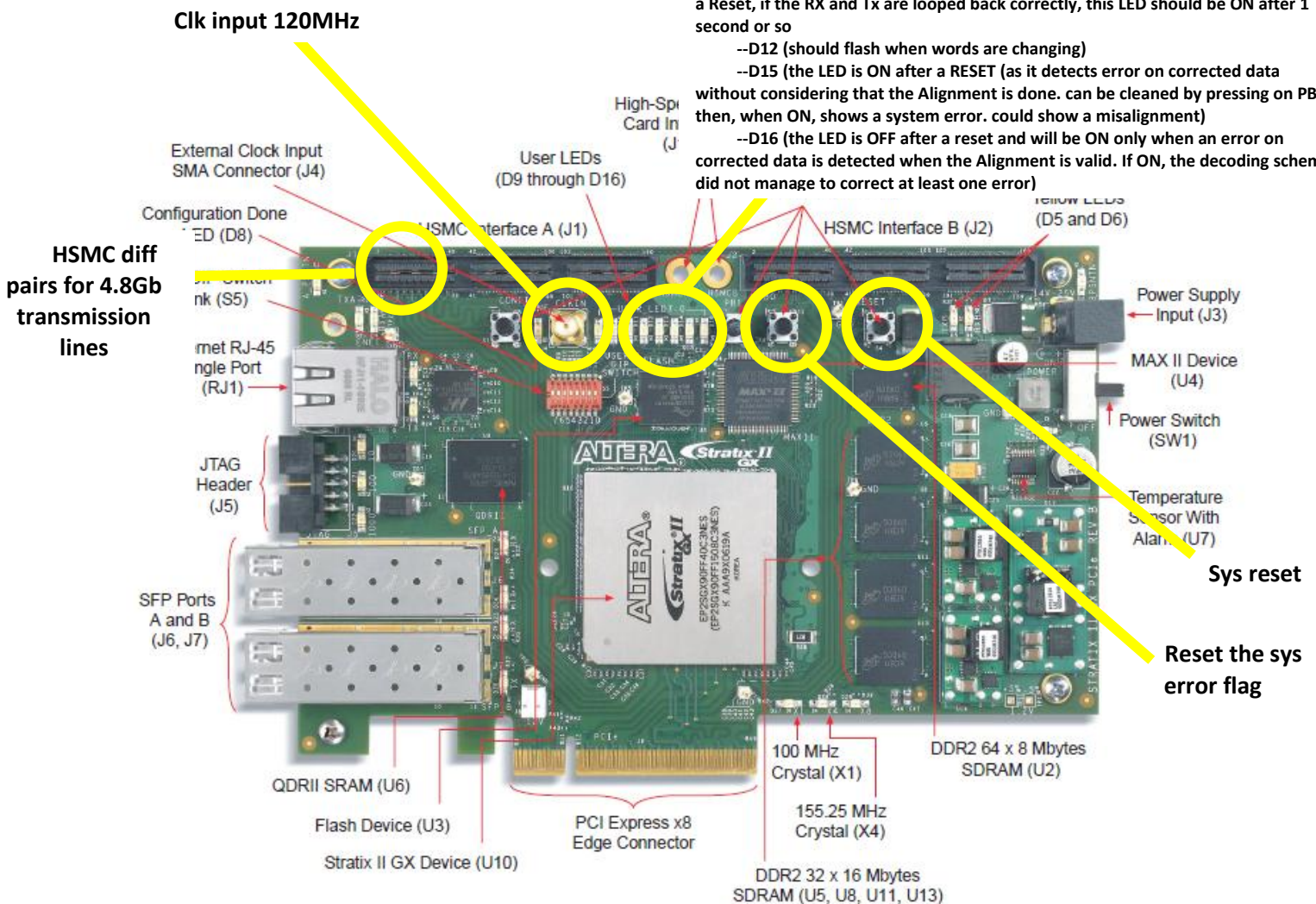
LEDs to quickly check the decoding process:

--D11. the LED is ON when the Received Data are Valid (Alignment Done). After a Reset, if the RX and Tx are looped back correctly, this LED should be ON after 1 second or so

--D12 (should flash when words are changing)

--D15 (the LED is ON after a RESET (as it detects error on corrected data without considering that the Alignment is done. can be cleaned by pressing on PB0. then, when ON, shows a system error. could show a misalignment)

--D16 (the LED is OFF after a reset and will be ON only when an error on corrected data is detected when the Alignment is valid. If ON, the decoding scheme did not manage to correct at least one error)



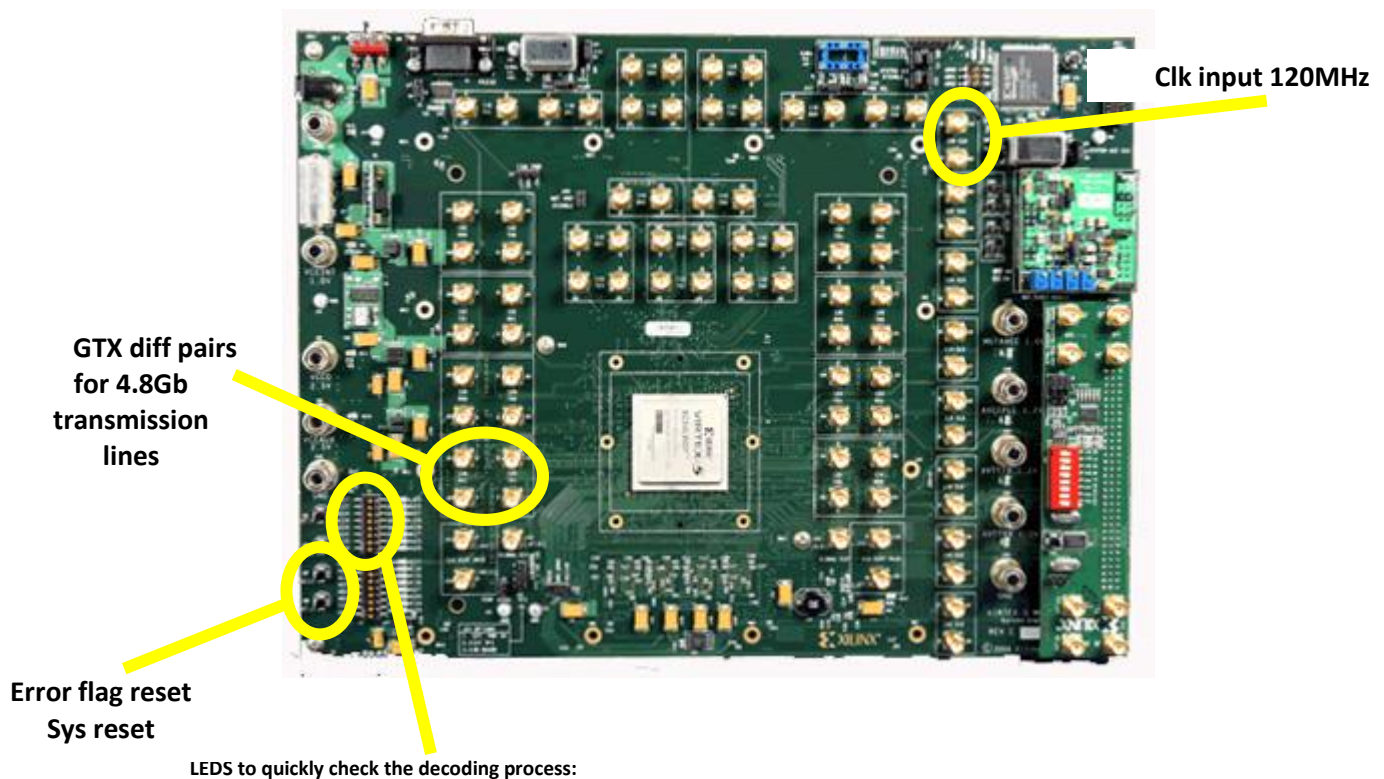
To rebuild the project for ISE (we are working with ISE 11.4), we have prepared a tcl script: open a cmd window and run the following commands :

```
cd your_project_path\Starter_kit\version-1.0.0\projects\Xilinx\Virtex5FXT\resource_optimization_with_multi_links
xtclsh resource_optimization_with_multi_links.tcl rebuild_project
```

The project should be fully recompiled from this only command. You can also open the project with ISE and recompile it manually.

Please note that the compilation is set for the device XC5VFX100T-3FF1136 and the power/pin assignments for the evaluation board type ML523. Be careful to redefine the power and pin assignments according to your own design.

Typical connection of the ML523 to test the GBT-FPGA Starter Kit:



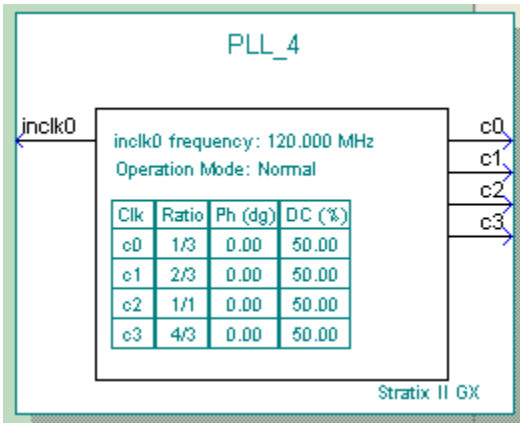
--AK27. the LED is ON when the Received Data are Valid (Alignment Done).  
After a Reset, if the RX and Tx are looped back correctly, this LED should be ON after 1 second or so  
--AK28 (should flash when words are changing)  
--AH27 (the LED is ON after a RESET (as it detects error on corrected data without considering that the Alignment is done. can be cleaned by pressing on PB0. then, when ON, shows a system error. could show a misalignment)  
--AJ26 (the LED is OFF after a reset and will be ON only when an error on corrected data is detected when the Alignment is valid. If ON, the decoding scheme did not manage to correct at least one error)



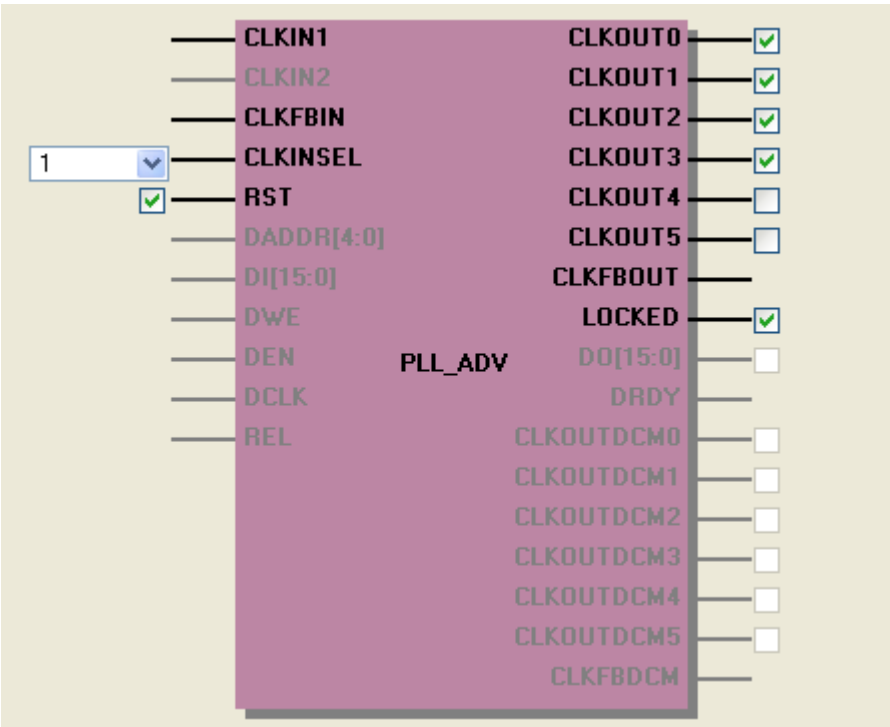
IP cores

PLL

The PLL entity is created using the Megacore Wizard (Altera) or the Core Generator (Xilinx). Its input frequency is 120MHz, and it delivers 40MHz, 80MHz, 120MHz and 160MHz. The PLL is vendor and device specific.



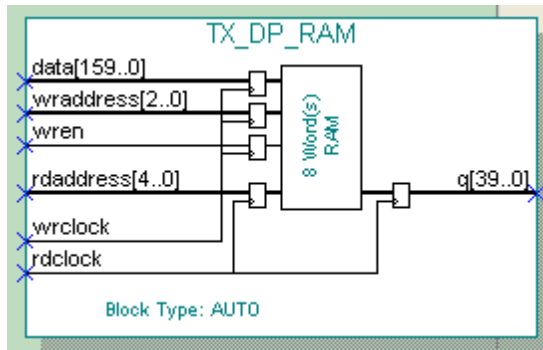
Altera PLL core



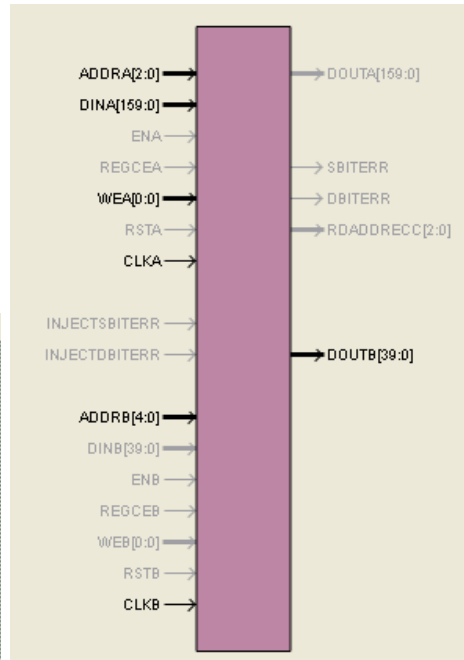
Xilinx PLL core



## TX\_DP\_RAM (used in Mux 120 to 40bits)

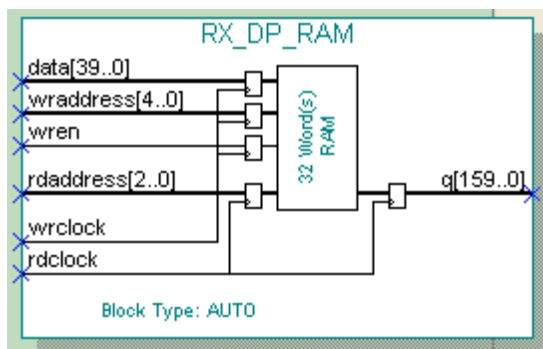


Altera Tx\_dp\_RAM core

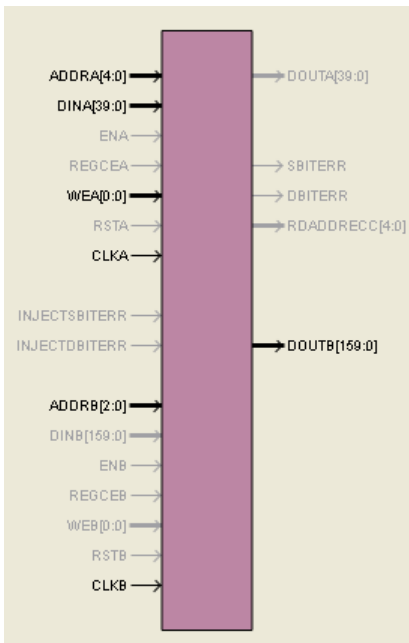


Xilinx Tx\_dp\_RAM core

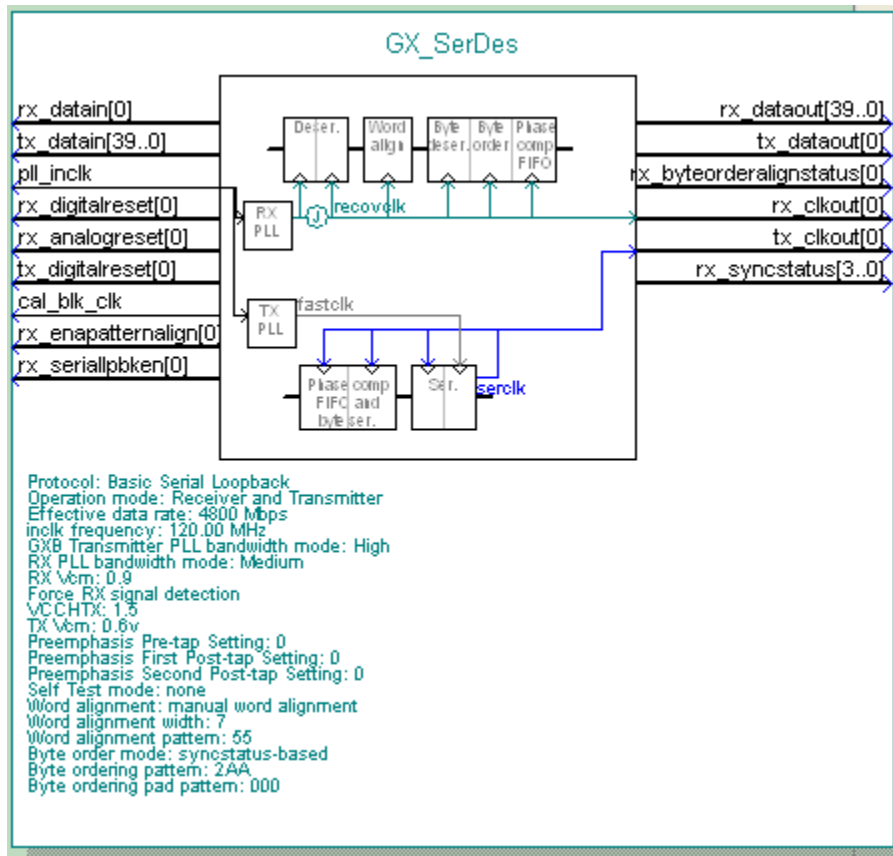
## RX\_DP\_RAM (used in demux 40 to 120 bits)



Altera Rx\_dp\_RAM core



Xilinx Rx\_dp\_RAM core



## Top file

The top file is a generic vhd file, allowing to implement as many transceivers as requested, with (for the moment) 3 types of optimization schemes. These parameters are declared in the Constants\_declaration.vhd file:

NUMBER\_OF\_LINKS: allows declaring the number of links to be implemented in your design

OPTIMIZE: specifies the optimization scheme.

0= no optimization

2= optimization by pairs (2 receivers share one RS decoder clocked at 2x40MHz)

3= optimization by 3 (3 receivers share one RS decoder clocked at 3x40MHz)

4= optimization by 4 (4 receiver share one RS decoder clocked at 4x40MHz – timing requirements are not met for all types of devices at that speed).

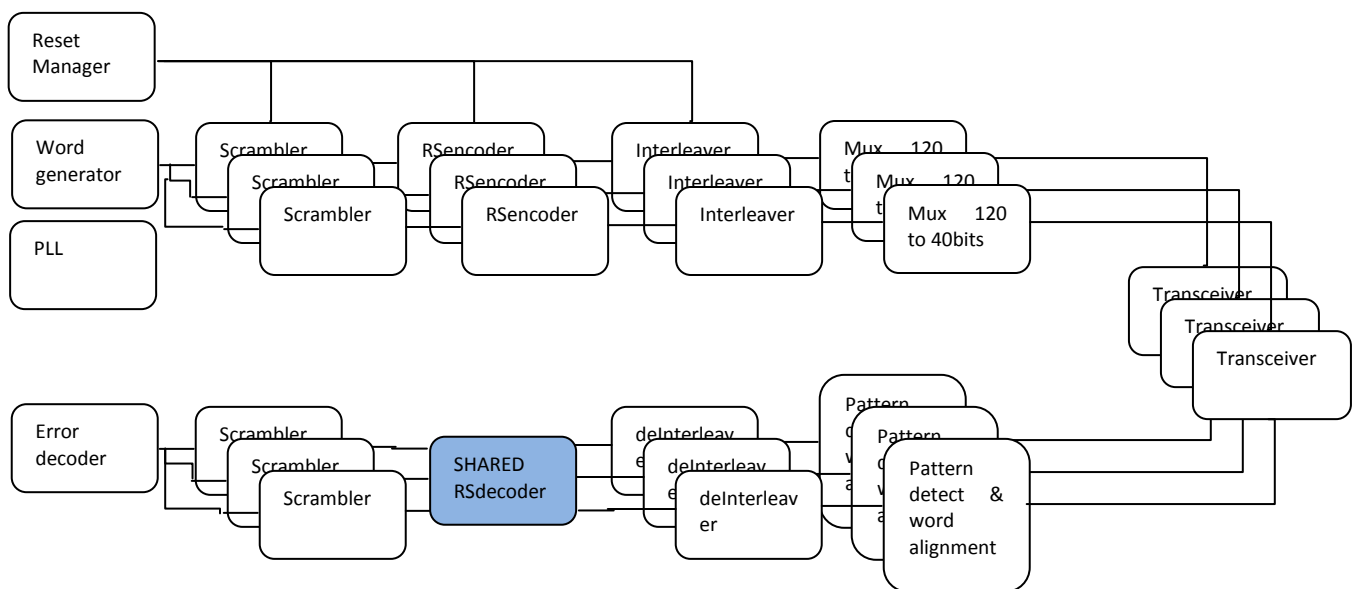
The top file is a linear instantiation of all the blocks required to build one or several links. According to the optimization type, the received (and de-interleaved frame) is multiplexed with frames of other links, passed through the RS decoder and de-multiplexed.

**For a simple link instantiation, choose**

**NUMBER\_OF\_LINKS=1**

**OPTIMIZE=0**

If OPTIMIZE≠0, you should have NUMBER\_OF\_LINKS/OPTIMIZE= integer.



This optimization scheme is working fine for ALTERA components, not yet for XILINX, as they need an optimization of their PLLs too, which is more complex.

***So, for Xilinx users, please use in 'constant\_declaration.vhd' the values:***

***NUMBER\_OF\_LINKS=1, OPTIMIZE=0.***

## Support policy

The GBT-FPGA design team will provide help to users for the use of the Starter Kit as is. The users are free to modify the code for their own application. However, in this case, we do not guaranty any support of the new code. Of course, we would be very happy to receive any comment, suggestion, bug report and we will try to maintain this kit up-to-date with technology changes (StratixIV, Virtex6). For any question, comments, report, please use the [gbt-fpga-users@cern.ch](mailto:gbt-fpga-users@cern.ch) mailing list. The members of this mailing list are both users and designers. This distinction only makes sense anyway at the start of this project, as the users will quickly become designers, and designers users!

**To become member of the GBT-FPGA users list, please send an email to [sophie.baron@cern.ch](mailto:sophie.baron@cern.ch), with a very short description of the project which you are working for, and why and how you intend to use the GBT core.**

## GBT community

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As mentioned above, a mailing list has been created, including all the registered users of the GBT-FPGA ([gbt-fpga-users@cern.ch](mailto:gbt-fpga-users@cern.ch)) to ease communication within the GBT FPGA users' community. All the emails sent to this mailing list are archived into the GBT-FPGA project website: <https://espace.cern.ch/GBT-Project/GBT-FPGA/Lists/GBTFPGA%20users%20exchange/AllItems.aspx>.

**To become member of the GBT-FPGA users list, please send an email to [sophie.baron@cern.ch](mailto:sophie.baron@cern.ch), with a very short description of the project which you are working for, and why and how you intend to use the GBT core.**

## Useful links

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### GBT project

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- GBT project main page: <https://espace.cern.ch/GBT-Project/default.aspx>
- GBT system integration: <https://espace.cern.ch/GBT-Project/GBTX/Specifications/Forms/AllItems.aspx>

### SVN documentation and tools

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- Documentation about SVN provided by CERN: <http://svn.web.cern.ch/svn/docs.php>
- SubVersion client for windows: <http://tortoisesvn.net/>

### GBT protocol

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- Choice of the GBT encoder scheme: <https://espace.cern.ch/GBT-Project/GBTX/Publications/thesis.pdf>

### GBT-FPGA project

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- GBT-FPGA main page: <https://espace.cern.ch/GBT-Project/GBT-FPGA/default.aspx>
- GBT-FPGA firmware releases:  
<https://espace.cern.ch/GBT-Project/GBT-FPGA/Lists/Starter%20Kit%20Firmware%20Releases/AllItems.aspx>
- GBT-FPGA Firmware bug tracking :  
<https://espace.cern.ch/GBT-Project/GBT-FPGA/Lists/Starter%20Kit%20Bug%20tracking/AllItems.aspx>

### GBT-FPGA original design team

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