Status of the upgrade work in Valencia

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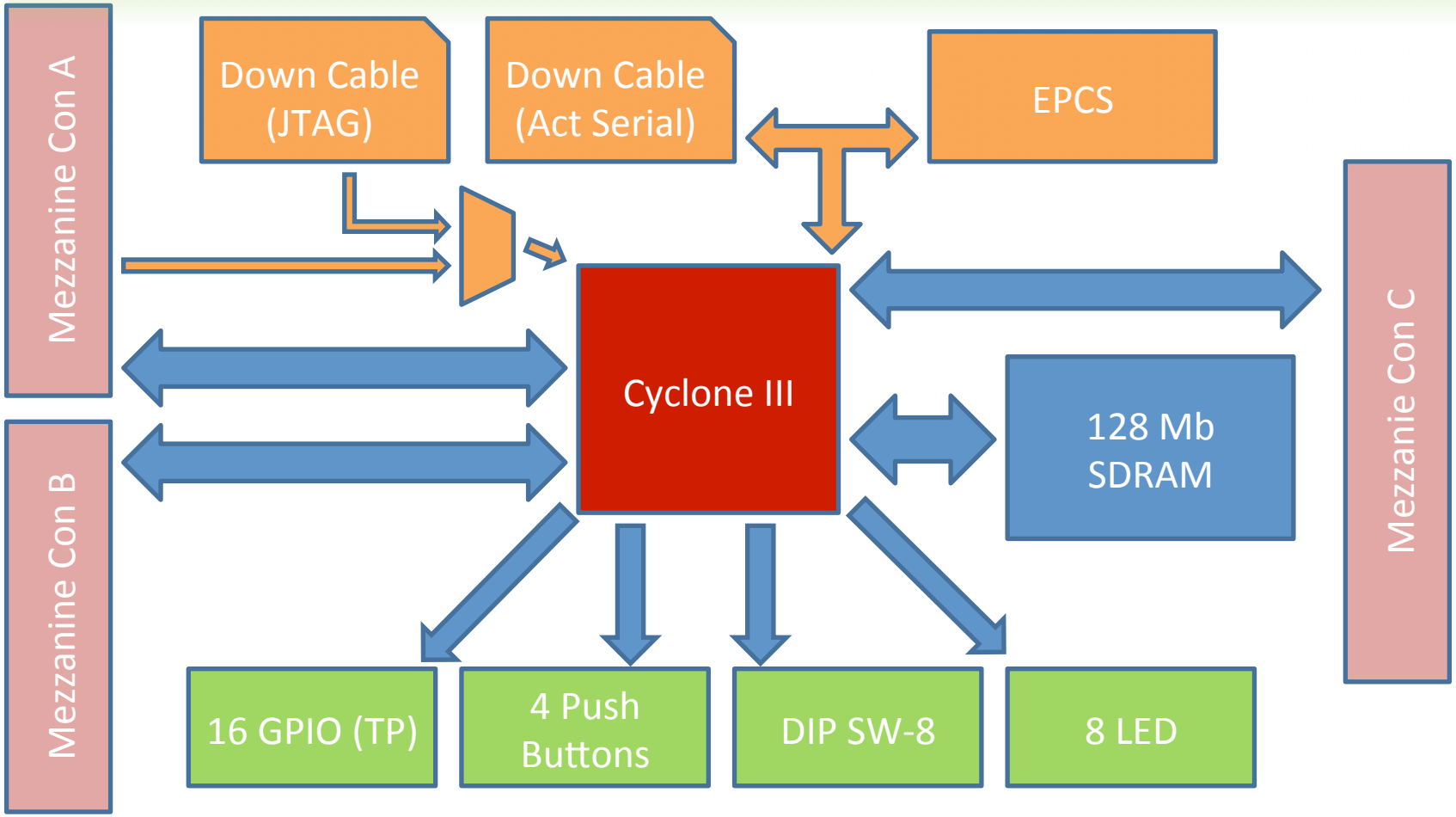
Design of a FPGA-based PU Mezzanine Card

Motivation

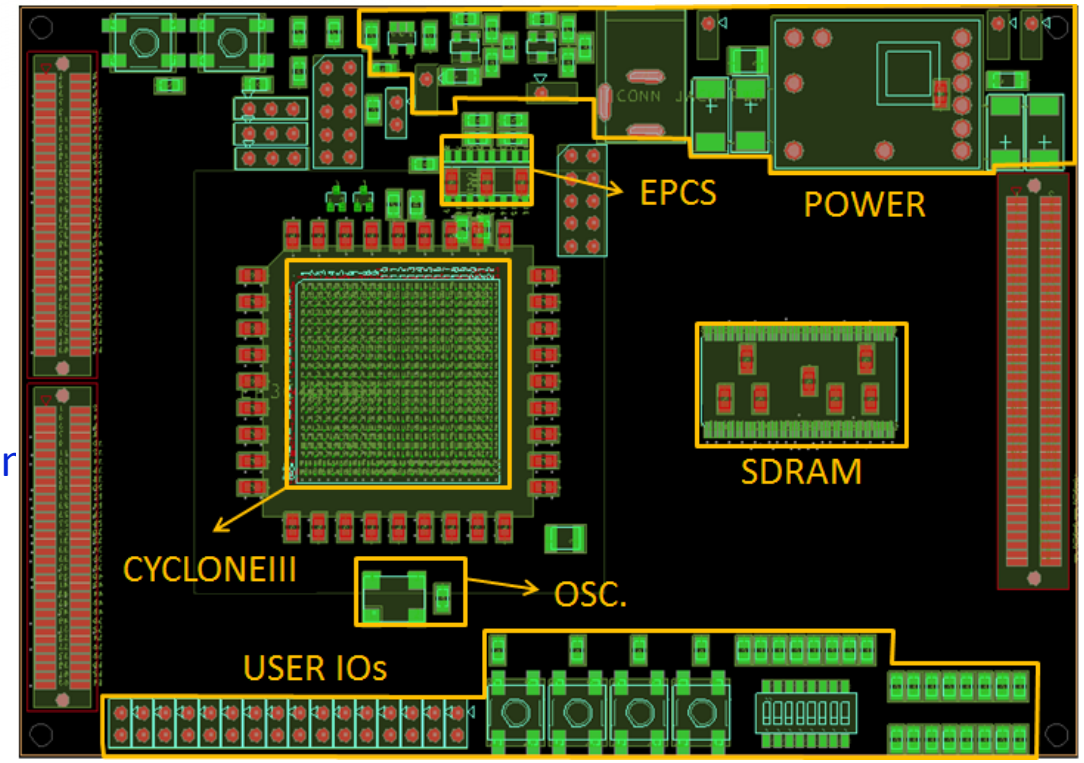
- Main goal: to develop a hardware platform to evaluate the performance of FPGAs in the implementation of OF using dedicated DSP blocks and explore extra capabilities like embedded processor systems to increase its functional possibilities.
- Its a prototype which let us gain some experience in the use of FPGAs for the current DSP PU tasks, as well as estimate its pros/cons in terms of performance, power consumption and complexity of the board.
- The platform will be a Mezzanine Card PU, based in a Altera Cyclone III and fully compatible with the present system.

The Cyclone III PU board



The Cyclone III PU board

- Cyclone III 40k 484 pin FPGA
- 128 Mbit SDRAM
- 64 Mbit EPCS flash
- 3 configuration schemes
- Standalone and plugged operating modes
- User IO: DIP switch, pushbuttons, leds and testpoir
- External 100 MHz oscillator
- 10 layers stack-up:
  - 6 signal layers
  - 4 power plane layers



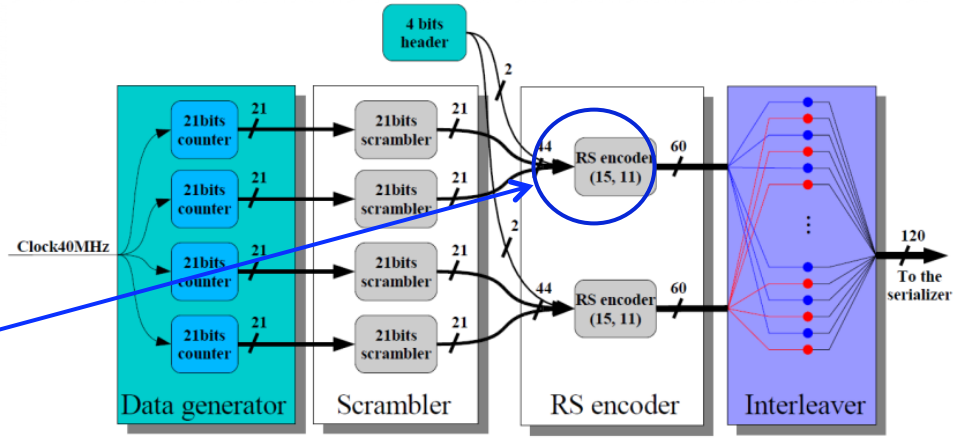
Status of the design

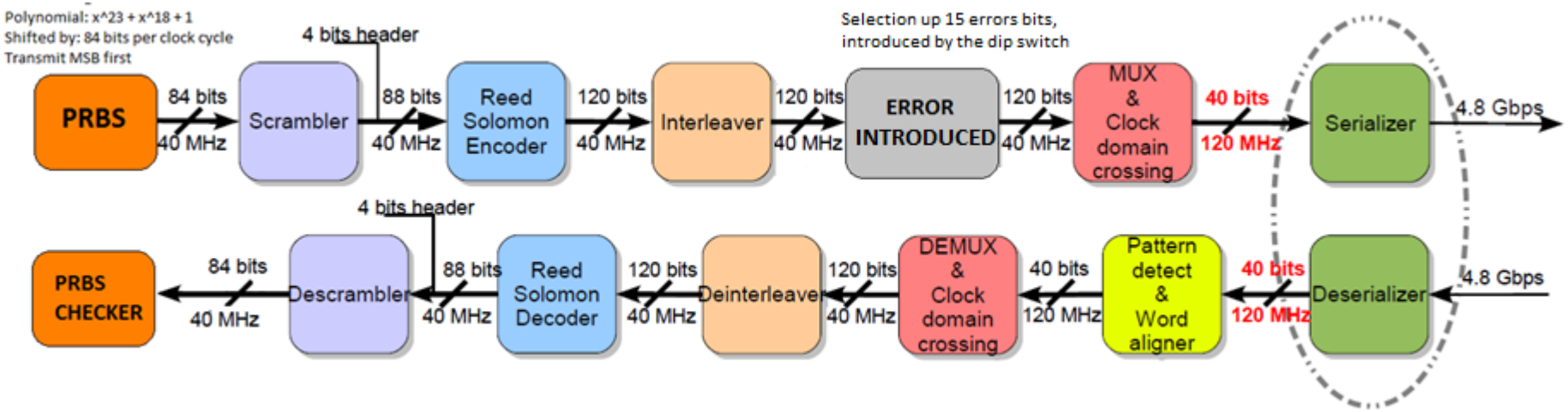
- ✓ Schematics
- ✓ Placement
- ✓ Stack-up, trace width and constraints definition
- Routing… 45%
- Manufacturing: June 2011
- Future work:
  - Electrical tests
  - Configuration tests
    - JTAG (standalone)
    - JTAG (motherboard)
    - Active Serial
  - Present system functional compatibility test
  - Extended functionality evaluation

GBT Activities

GBT Error correction tests

- PRBS generator & checker implemented:
  - Polynomial $X^{23}+X^{18}+1$
  - 84bits@40MHz
  - Errors introduced in transmission chain (1 RS encoder)



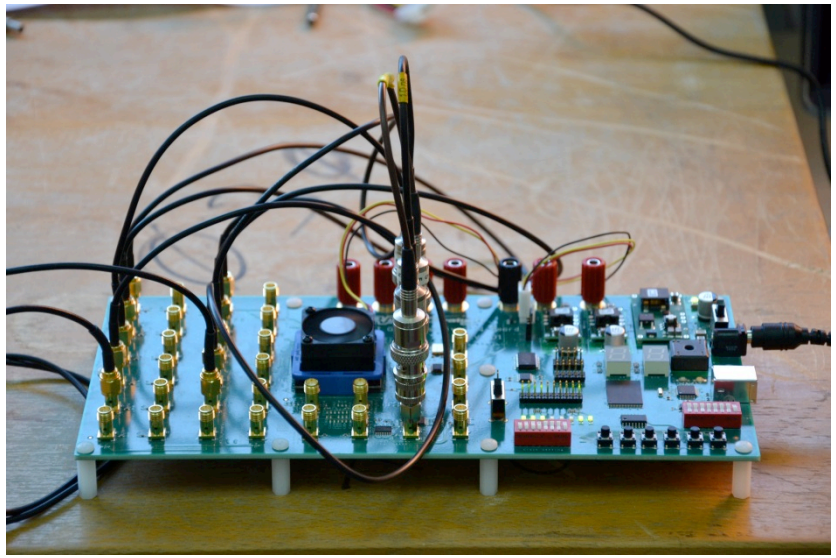


GBT Error correction tests

Preliminary results:

# DATA BITS CHANGED ON RS Encoder1	Status	# FEC BITS CHANGED to obtain error
1	Corrected	5
2	Corrected	2 and > 4
3	Corrected	4
4	Corrected	5
5	Corrected	4
6	Corrected	2 or > 3
7	Corrected	1
8	Corrected	1
9	Not corrected	0
10	Not corrected	0
11	Not corrected	0
12	Not corrected	0
13	Not corrected	0
14	Not corrected	0
15	Not corrected	0

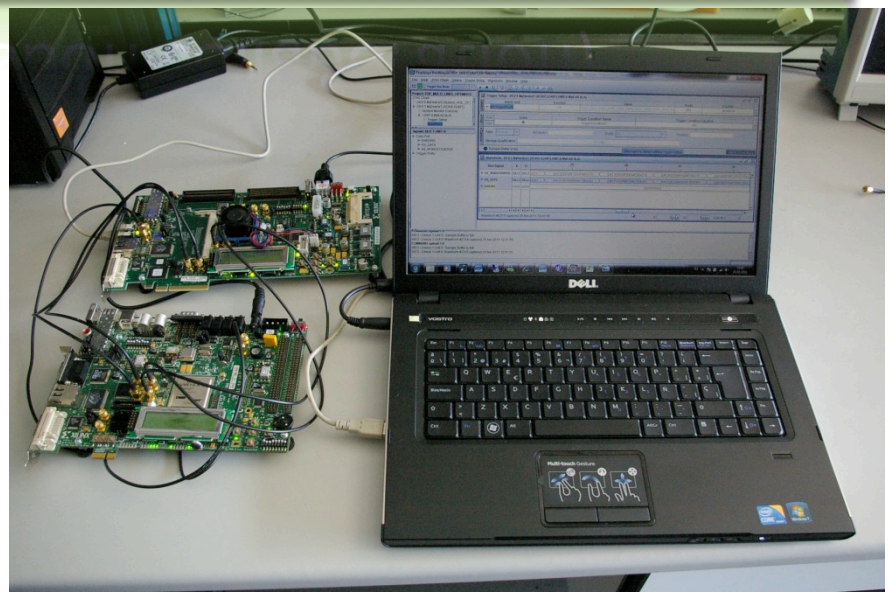
Conclusion: GBT protocol meets its specifications correcting up to 8 consecutive corrupted bits per RS block

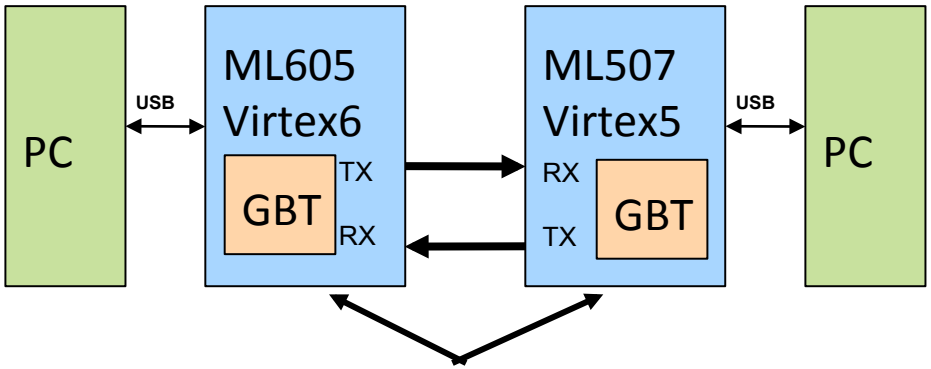


Tested 6 GBT links with 8 bit errors per encoder for 24 hours.

Communication tests: inter-board and board-to-board (Valencia – Lisbon collaboration)

- ML605-Virtex-6 and ML507-Virtex-5 working full-duplex with no errors
  - Common clock from either board
  - Different clock from Stratix II GX Board
- Loopback GBT TX-RX implementation in Virtex-6 (up to 12 GBT links)
- Advantage of Virtex-6 over Virtex-5: transceiver instantiation is individual (less waste of resources)

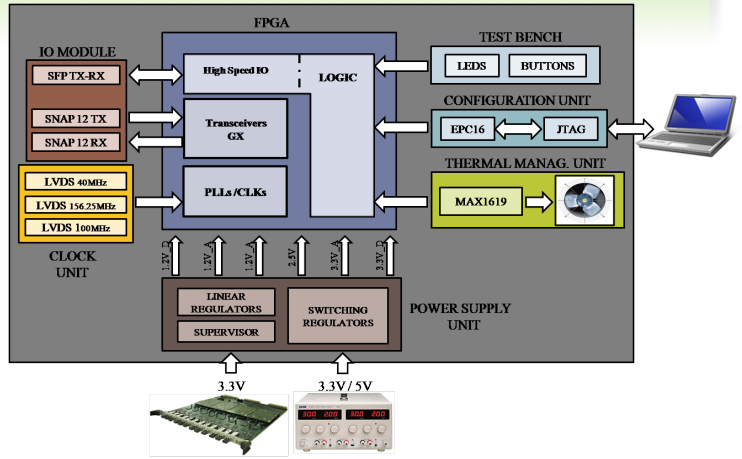




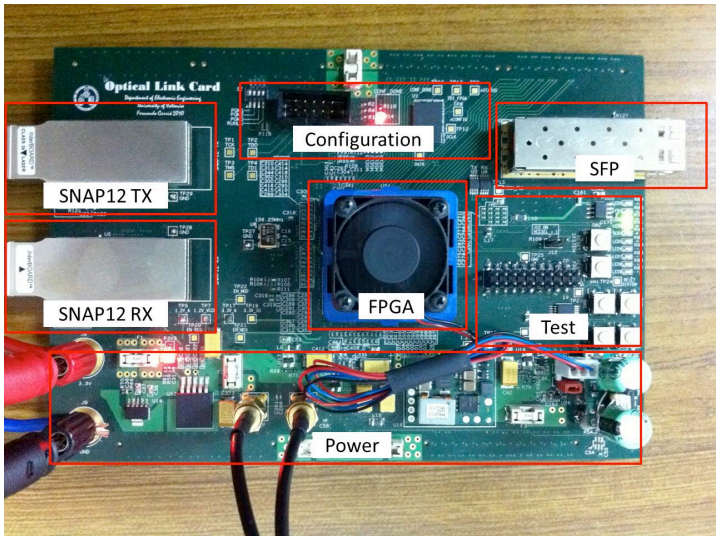
Optical Link Card status

Optical Link Card - Overview

- Main devices:
  - SNAP12 Transmitter/Receiver module (Link up to 75 Gbps)
    - SN-T12-C01001 / SN-R12-C01001
  - SFP module (Link up to 1 Gbps)
    - V23818-M305-B57
  - Altera Stratix II GX with 12 GX transceivers
    - EP2SGX60E
- Physical card features:
  - Size: 2 x PU position in ROD (174mm x 120mm)
  - 12 layers
    - 6 power planes
    - 6 signal layers
- Status:
  - Electrical test done
  - Maximum data bandwidth achieved
    - Total bandwidth 75Gbps
    - 6.25Gbps per channel
  - GBT protocol implemented successfully



Block diagram



Optical Link Card

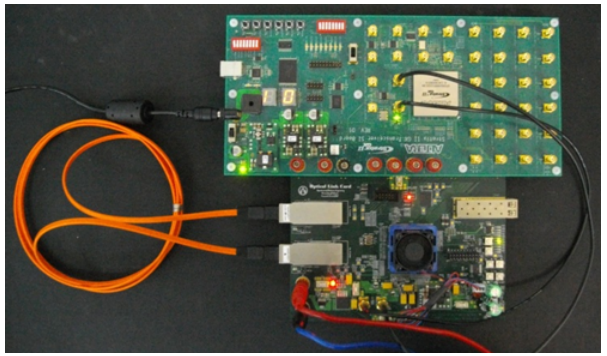
OLC Tests

- Maximum data bandwidth
  - Raw data: 32 bit counter without protocol
  - 6.25Gbps per fiber
  - Data correlation with Altera Signal Tap
  - Total measured bandwidth of 75Gbps
  - Power consumption 11.71 W

OLC	1 GBT link
ALUTs	1976
	4%
Dedicated Logical Registers	1680
	3%
Block Memory bits	2560
	0.1%
PLLs	1
	12.5%

Resource occupation for 1 GBT link

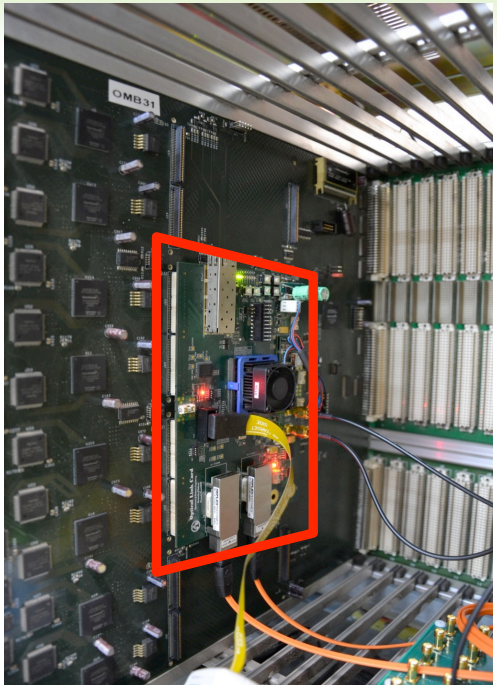
- 1 link GBT protocol implementation
  - Power supply from external supply
  - Receiver and transmitter located in different GX transceiver block
  - 48 hours without errors
  - BER of $3.61 \cdot 10^{-15}$ with a confidence of 95%
  - Data rate of 4.8Gbps
  - Power consumption 7.128 W



OLC running 1 link GBT

OLC Tests

- 12 links GBT protocol implementation
  - 12 link GBT protocol
  - Power supply from OMB
  - Receiver and transmitter located in different GX transceiver block
  - 24 hours without errors
  - Internal FIFO compensation needed
    - Due to violated setup and hold internal times
  - BER of $6.05 \cdot 10^{-16}$ with a confidence of 95%
  - Total bandwidth of 57.6Gbps
  - Power consumption 14.025 W



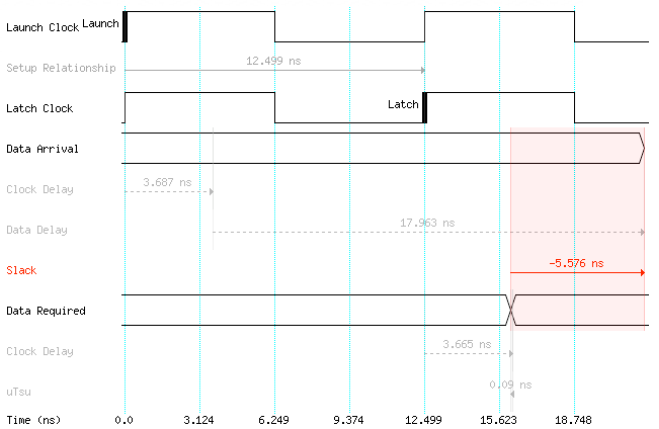
OLC connected to OMB running 12 GBT links at 175

OLC	12 GBT links
ALUTs	22953
	47%
Dedicated Logical Registers	15917
	33%
Block Memory bits	30720
	1.2%
PLLs	1
	12.5%

Resource occupation for 12 GBT links

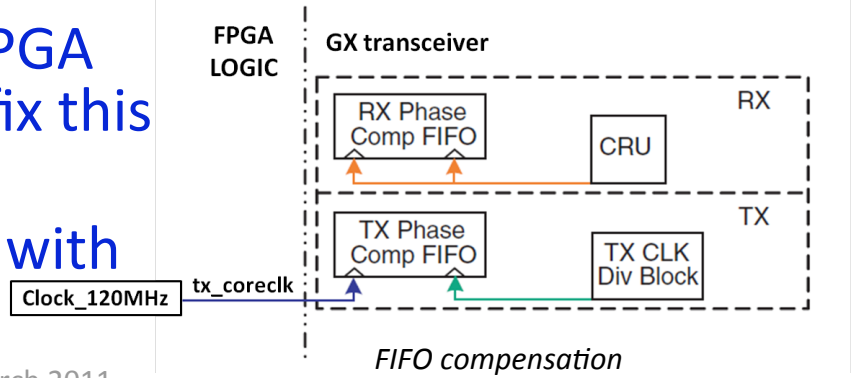
GBT implementation in OLC

- FPGA internal timing problems
  - Setup and hold times not meet requirements
  - Errors due to non-synchronization between logic and GX transceivers
  - Timing problems increase with the number of GBT links implemented



Violated setup timing diagram

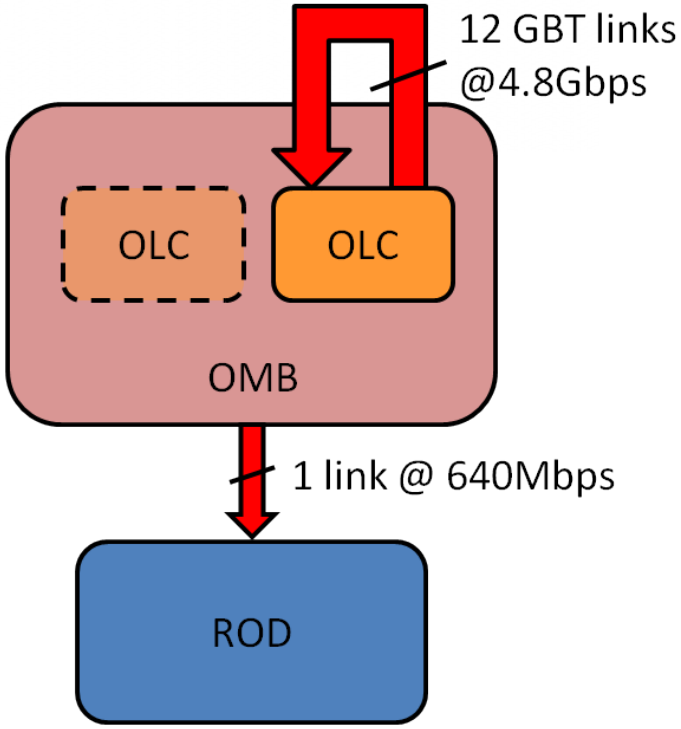
- Solved with FIFO compensation
  - FIFO compensation between FPGA logic clock and GX transmitter fix this problem in OLC
  - Timing requirements not meet with GBT optimization



FIFO compensation

Work ongoing - OLC working with ROD

- Test assembly
  - OLC connected to OMB as PU
  - OLC with SNAP12 connectors in loopback
  - OMB connected to ROD with G-link
- OLC purpose
  - Simulate Front End data and sends it to SNAP12 loopback
  - Send received simulated Front End data to OMB with Mezzanine connectors
- OMB purpose
  - Send simulated Front End data to ROD with a G-link channel



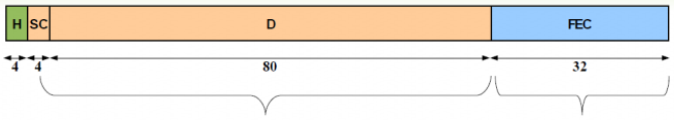
OLC working with ROD scheme

Thank you for your time

Backup Slides

GBT Error correction tests

	ERROR INTRODUCED		INTERLEAVER OUTPUT	
Output	119	116 <=	119	116 HEADER
Output	115	112 <=	59	56 DATA RS1
Output	111	108 <=	115	112 DATA RS2
Output	107	104 <=	55	52 DATA RS1
Output	103	100 <=	111	108 DATA RS2
Output	99	96 <=	51	48 DATA RS1
Output	95	92 <=	107	104 DATA RS2
Output	91	88 <=	47	44 DATA RS1
Output	87	84 <=	103	100 DATA RS2
Output	83	80 <=	43	40 DATA RS1
Output	79	76 <=	99	96 DATA RS2
Output	75	72 <=	39	36 DATA RS1
Output	71	68 <=	95	92 DATA RS2
Output	67	64 <=	35	32 DATA RS1
Output	63	60 <=	91	88 DATA RS2
Output	59	56 <=	31	28 DATA RS1
Output	55	52 <=	87	84 DATA RS2
Output	51	48 <=	27	24 DATA RS1
Output	47	44 <=	83	80 DATA RS2
Output	43	40 <=	23	20 DATA RS1
Output	39	36 <=	79	76 DATA RS2
Output	35	32 <=	19	16 DATA RS1
Output	31	28 <=	75	72 FEC RS2
Output	27	24 <=	15	12 FEC RS1
Output	23	20 <=	71	68 FEC RS2
Output	19	16 <=	11	8 FEC RS1
Output	15	12 <=	67	64 FEC RS2
Output	11	8 <=	7	4 FEC RS1
Output	7	4 <=	63	60 FEC RS2
Output	3	0 <=	3	0 FEC RS1



H: Header, 4 bits
SC: Slow Control 4 bits
GBT control 2 bits (80 Mb/s)
Slow control 2 bits (80 Mb/s)
D: Data (3.2 Gbps)
FEC: Forward Error Correction (32 bits)

Bits to be changed in order to emulate transmission burst errors:

Up to 8 data bits and 7 FEC bits

Speed estimates in Virtex-6 for selected examples (ISE 12.4 IDE)

- Combinatoric Modules: **4 x Reed-Solomon Decoder** (4 modules is maximum possible due to # I/O pins.) Critical I/O path: 2.212 ns.
- Sequential module: **1 x Scrambler**. Max. clock frequency ~800 MHz; delay 1.25 ns.

```
================================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 3504 / 480
--------------------------------------------------------------------------------
Delay:               2.212ns (Levels of Logic = 4)
  Source:            Input_o<56> (PAD)
  Destination:       Output_0<73> (PAD)

  Data Path: Input_o<56> to Output_0<73>
                                Gate     Net
    Cell:in->out      fanout   Delay    Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             16   0.003   0.876  Input_o_56_IBUF
(Input_o_56_IBUF)
     LUT6:I0->O             1   0.068   0.775  transceivers_instantiation
[0].Inst_Encoding/RSEncoder_83_42/polydivider_inst/net<82><1>12
(transceivers_instantiation[0].Inst_Encoding/RSEncoder_83_42/
polydivider_inst/net<82><1>11)
     LUT6:I1->O             4   0.068   0.419  transceivers_instantiation
[0].Inst_Encoding/RSEncoder_83_42/polydivider_inst/net<82><1>14
(Output_0_73_OBUF)
     OBUF:I->O                  0.003          Output_0_73_OBUF
(Output_0<73>)
    ----------------------------------------
    Total                       2.212ns (0.142ns logic, 2.070ns route)
                                        (6.4% logic, 93.6% route)
================================================================================
```

```
================================================================================
Timing constraint: Default period analysis for Clock 'Clock'
  Clock period: 1.249ns (frequency: 800.641MHz)
  Total number of paths / destination ports: 536 / 168
--------------------------------------------------------------------------------
Delay:               1.249ns (Levels of Logic = 1)
  Source:            Scrambler_20_0/FREG_20 (FF)
  Destination:       Temp_Output_20 (FF)
  Source Clock:      Clock rising
  Destination Clock: Clock rising

  Data Path: Scrambler_20_0/FREG_20 to Temp_Output_20
                                Gate     Net
    Cell:in->out      fanout   Delay    Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FD:C->Q                4   0.375   0.795  Scrambler_20_0/FREG_20
(Scrambler_20_0/FREG_20)
     LUT5:I0->O             1   0.068   0.000  Scrambler_20_0/dout_s<21>1
(Scrambled_Word<20>)
     FDC:D                      0.011          Temp_Output_20
    ----------------------------------------
    Total                       1.249ns (0.454ns logic, 0.795ns route)
                                        (36.3% logic, 63.7% route)
================================================================================
```

Virtex-6 resources vs. # of full GBT links compiled in the device

	1 LINK		2 LINKS		**12 LINKS**		Total Res.
# Slice Registers	734	0.24%	1382	0.46%	**7818**	**2.59%**	301440
# Slice LUTs	2045	1.36%	4084	2.71%	**22336**	**14.82%**	150720
# occupied slices	726	1.93%	1384	3.67%	**8473**	**22.49%**	37680
# RAMB36E1	4	0.96%	8	1.92%	**48**	**11.54%**	416
# RAMB18E1	21	2.52%	42	5.05%	**152**	**18.27%**	832
# GTXE1s	1	5.00%	2	10.00%	**12**	**60.00%**	20